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Jameco Part Number
40416

Am2817A

2048 x 8-Bit Electrically Erasable PROM

DISTINCTIVE CHARACTERISTICS

- 5-Volt-only operation
- Write-protect circuitry to preserve data on power up and power down
- Ready/$\overline{\text{Busy}}$ pin for end-of-write indication
- Self-timed write cycle with on-chip latches
- Minimum endurance of 10,000 write cycles per byte with a 10-year retention. For detailed information, see the Am9864 Reliability Report (PID #06891A)

GENERAL DESCRIPTION

The Am2817A is a 16,384-bit Electrically Erasable Programmable Read-Only Memory (EEPROM). It is organized as 2048 words by 8 bits per word and offers a fast 200 ns read access time.

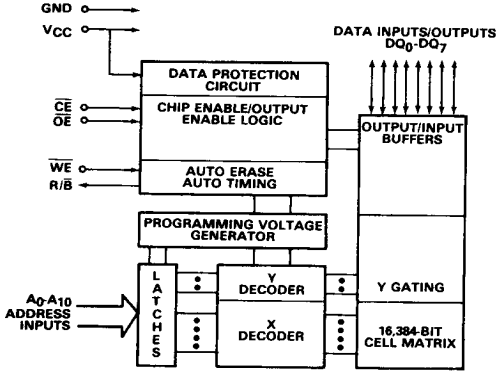
The 2817A has a fully self-timed write cycle with address, data, and control lines latched during the write operation.

The latched inputs and self-timed write cycle free the microprocessor to perform other processes during write. A transparent automatic erase before write enhances system performance.

To eliminate bus contention in a microprocessor system, this device offers separate Output Enable ($\overline{\text{OE}}$) and Chip Enable ($\overline{\text{CE}}$) controls.

The Am2817A is fabricated on AMD's highly manufacturable N-Channel silicon gate process and uses AMD's proprietary EEPROM technology to achieve electrically alterable, non-volatile storage.

BLOCK DIAGRAM



BD003532

MODE SELECT TABLE

$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Outputs	R/$\overline{\text{B}}$	Mode
L	L	H	D_{OUT}	Hi-Z	Read
L	H	H	Hi-Z	Hi-Z	Read Inhibit
H	X	X	Hi-Z	Hi-Z	Standby
L	H	⊓	D_{IN}	⊓	Byte Write
Automatic before each "Write"					Byte Erase
X	L	X	–	–	Write Inhibit

H = HIGH
L = LOW
X = Don't Care
⊓ = Pulse

PRODUCT SELECTOR GUIDE

Part Number	Am2817A-2	Am2817A-20	Am2817A	Am2817A-25	Am2817A-3	Am2817A-35
Access Time	200 ns		250 ns		350 ns	
Supply Tolerance	±5%	±10%	±5%	±10%	±5%	±10%

Publication # 06153 Rev. D Amendment /0
Issue Date: May 1986

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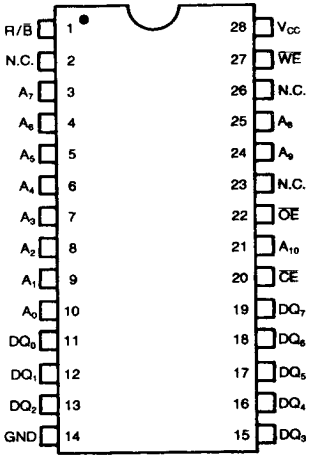
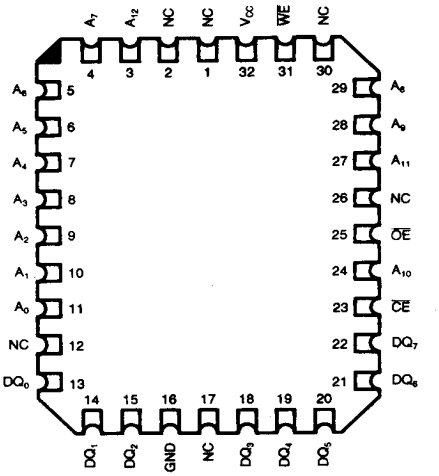
CONNECTION DIAGRAMS
Top View



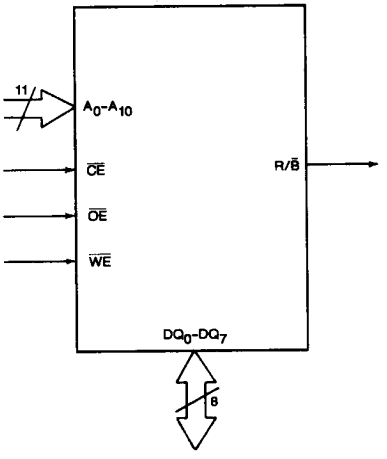
CD005372



CD006001

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002273

V_{CC} = Power Supply
GND = Ground

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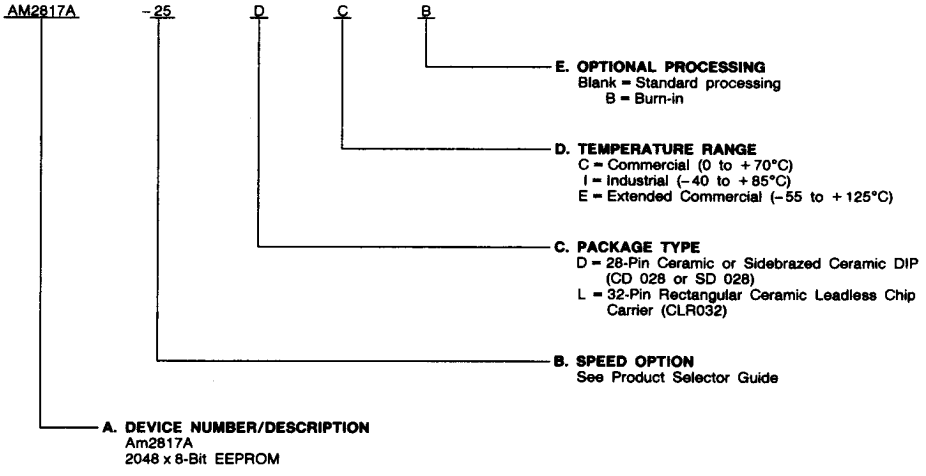
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM2817A-2	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2817A-20	
AM2817A	
AM2817A-25	
AM2817A-3	
AM2817A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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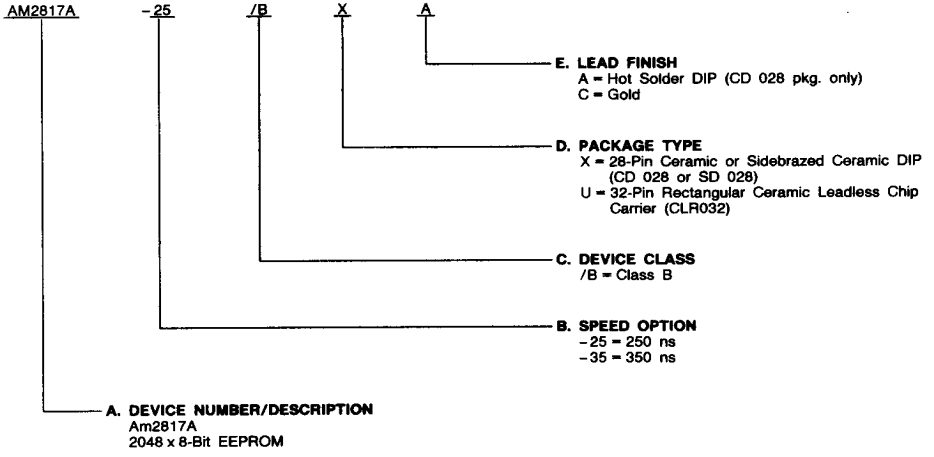
ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM2817A-25	/BXA, /BXC, /BUC
AM2817A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

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FUNCTIONAL DESCRIPTION

Read Mode

The Am2817A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am2817A has a standby mode which reduces the active power dissipation by 60% from 500 mW to 200 mW (values for 0 to 70°C). The Am2817A is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Data Protection

The Am2817A incorporates several features that prevent unwanted write cycles during V_{CC} power-up and power-down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.8 volts. It is the user's responsibility to insure that the control levels are logically correct when V_{CC} is above 3.8 volts.

There is a $\overline{WE}$ lockout circuit that prevents $\overline{WE}$ pulses of less than 10 ns* duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

Write Mode

The Am2817A has a write cycle that is similar to that of a static RAM. The write cycle is completely self timed, and initiated by a LOW-going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ (R/$\overline{B}$) pin goes to a logic-LOW level indicating that the Am2817A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When R/$\overline{B}$ goes back to a HIGH, the Am2817A has completed writing and is ready to accept another cycle.

Output OR-Tieing

To accommodate mulitiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Ready/$\overline{Busy}$ Pin

The Ready/$\overline{Busy}$ (R/$\overline{B}$) pin is an open-drain output which allows two or more R/$\overline{B}$ signals to be OR-tied together. The value of the pullup resistor required is as follows:

$$R_{pu} = \frac{4.6\ V}{2.1\ mA - I_{IL}}$$

I_{IL} = total V_{IL} input current of devices connected to R/$\overline{B}$.

A typical pullup resistor value for R/$\overline{B}$ is 3 kΩ, assuming I_{IL} is less than 0.5 mA.

APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

* This parameter is sampled and not 100% tested.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied ..... −65 to +135°C
Voltage on All Inputs with Respect to GND ..... +6.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC} ±5%) ..... +4.75 to +5.25 V
(V_{CC} ±10%) ..... +4.50 to +5.50 V

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC} ±10%) ..... +4.50 to +5.50 V

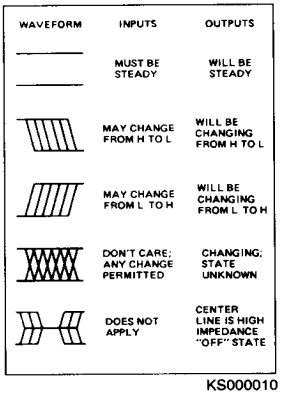
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.5 V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.5 V			10	µA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}			40	mA
I_{CC2}	V_{CC} Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}			100	mA
I_{CC}	V_{CC} Current (Write)	$\overline{WE}$ ⊓, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			100	mA
V_{IL}	Input LOW Voltage		−0.1		.8	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 1	Volts
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			.45	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA	2.4			Volts
V_{WI}	Write Inhibit Voltage		3.3	3.8		Volts
V_{RB}	R/$\overline{B}$ Output LOW	I_{RB} = 2.1 mA			.45	Volts
C_{IN}	Input Capacitance (Notes 1, 2 & 3)	V_{IN} = 0 V		4	10	pF
C_{OUT}	Output Capacitance (Notes 1, 2 & 3)	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, V_{OUT} = 0 V		8	12	pF

Notes 1. This parameter is sampled on a periodic basis and not 100% tested.
2. Freq. = 1 MHz @ 25°C.
3. Typical values are for nominal supply voltages.

KEY TO SWITCHING WAVEFORMS


WAVEFORM
INPUTS
OUTPUTS
MUST BE STEADY
WILL BE STEADY
MAY CHANGE FROM H TO L
WILL BE CHANGING FROM H TO L
MAY CHANGE FROM L TO H
WILL BE CHANGING FROM L TO H
DON'T CARE; ANY CHANGE PERMITTED
CHANGING; STATE UNKNOWN
DOES NOT APPLY
CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

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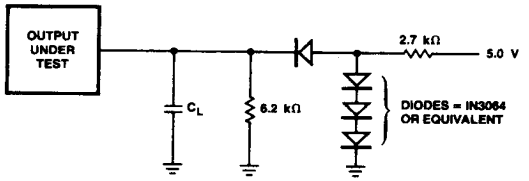
Switching Test Conditions

Output load: 1 TTL gate and C_L = 100 pF
Input pulse levels: 0.45 V to 2.4 V

Timing Measurements Reference Levels

Input: 0.8 V and 2.0 V
Output: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



TC002491

C_L = 100 pF, including jig capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameter Symbol	Parameter Description	Test Conditions		Am2817A-2, Am2817A-20 Min.	Am2817A-2, Am2817A-20 Max.	Am2817A, Am2817A-25 Min.	Am2817A, Am2817A-25 Max.	Am2817A-3, Am2817A-35 Min.	Am2817A-3, Am2817A-35 Max.	Units
READ											
1	t_{ACC} (Note 3)	Address to Output Delay	$\overline{WE}$ = V_{IH} Output Load: 1 TTL gate and C_L = 100 pF Input Rise and Fall Times: ≤ 20 ns Input Pulse Levels: 0.45 to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2 V Outputs: 0.8 V and 2 V	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200		250		350	ns
2	t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE}$ = V_{IL}		200		250		350	ns
3	t_{OE} (Note 3)	Output Enable to Output Delay		$\overline{CE}$ = V_{IL}		75		100		120	ns
4	t_{DF} (Notes 1 & 4)	Output Enable HIGH to Output Float		$\overline{CE}$ = V_{IL}	0	60	0	60	0	80	ns
5	t_{OH} (Note 1)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First		$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		ns
WRITE											
6	t_{AS}	Address to Write Setup Time			20		20		20		ns
7	t_{CS}	$\overline{CE}$ to Write Setup Time			30		30		30		ns
8	t_{WP}	Write Pulse Width			100		100		100		ns
9	t_{AH}	Address Hold Time			50		50		50		ns
10	t_{DS}	Data Setup Time			50		50		50		ns
11	t_{DH}	Data Hold Time			20		20		20		ns
12	t_{CH}	$\overline{CE}$ Hold Time			0		0		0		ns
13	t_{OES}	$\overline{OE}$ Setup Time			20		20		20		ns
14	t_{OEH}	$\overline{OE}$ Hold Time			35		35		35		ns
15	t_{DB}	Time to Device Busy				100		100		100	ns
16	t_{WR}	Bytes Write Cycle				10		10		10	ms
17	t_{WPH}	Write Control Recovery			50		50		50		ns
18	t_{RE}	Write Recovery Time (Note 6)			0		0		0		ns
19	t_{RBO}	R/$\overline{B}$ to Output Time (Notes 2 & 6)				50		50		50	ns
20	t_{WEH} (Note 6)	$\overline{WE}$ HIGH Recovery from R/$\overline{B}$			10		10		10		μs
	(Notes 1 & 5)	Number of Writes per Byte			10		10		10		x1000

Notes: 1. This parameter is sampled on a periodic basis to worst-case test conditions and not 100% tested.
2. If $\overline{CE}$ and $\overline{OE}$ = V_{IL} when R/$\overline{B}$ is going to V_{OH}, then DQ_{0-7} becomes valid after t_{RBO} + t_{ACC} ns.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, which ever occurs first.
5. See Am9864 Reliability Report (PID #06891A).
6. This parameter is for information only. It is not tested nor characterized.

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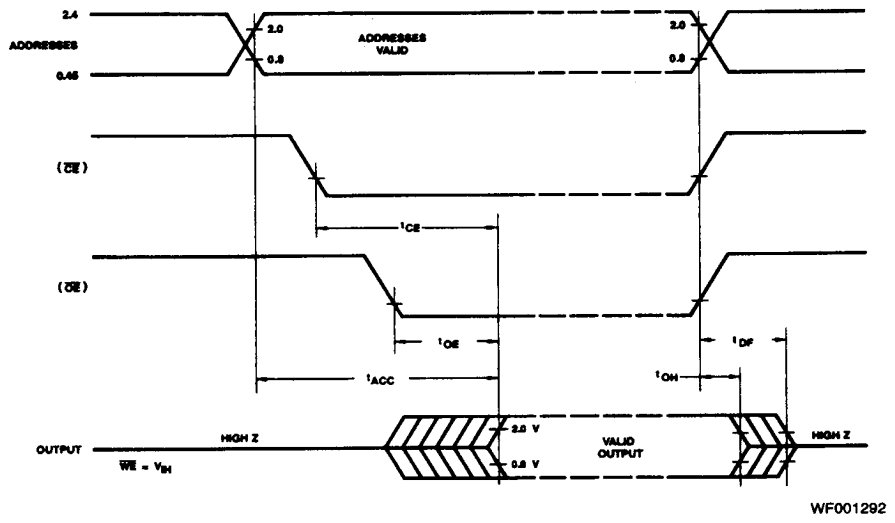
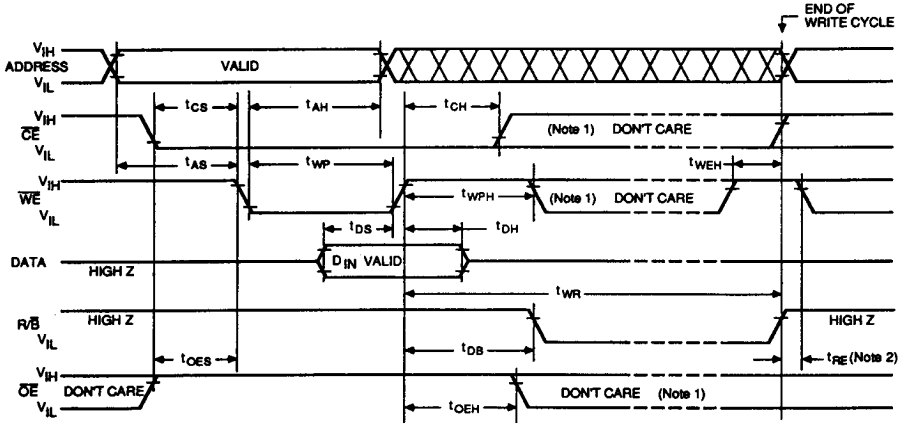
SWITCHING WAVEFORMS



WF001292

Read

Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.



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Write

Notes: 1. After t_{WPH} and before the end of the Write cycle (R/$\overline{B}$ goes HIGH), $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ are Don't Cares. However, in order to prevent an accidental write when R/$\overline{B}$ returns HIGH, it is recommended that at least one of the following conditions after t_{WPH}: $\overline{WE}$ HIGH, $\overline{CE}$ HIGH, or $\overline{OE}$ LOW.
2. After the Write cycle is completed (R/$\overline{B}$ HIGH), the user must meet one of the following conditions: $\overline{OE}$ LOW, $\overline{CE}$ HIGH, or $\overline{WE}$ HIGH.

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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups
I_{IL}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{CC}	1, 2, 3
V_{IL}	1, 2, 3
V_{IH}	1, 2, 3
V_{OL}	1, 2, 3
V_{OH}	1, 2, 3
V_{WI}	7, 8
V_{RB}	1, 2, 3
C_{IN}	4
C_{OUT}	4

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups	No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11	9	t_{AH}	9, 10, 11
2	t_{CE}	9, 10, 11	10	t_{DS}	9, 10, 11
3	t_{OE}	9, 10, 11	11	t_{DH}	9, 10, 11
4	t_{DF}	9, 10, 11	12	t_{CH}	9, 10, 11
5	t_{OH}	9, 10, 11	13	t_{OES}	9, 10, 11
6	t_{AS}	9, 10, 11	14	t_{OEH}	9, 10, 11
7	t_{CS}	9, 10, 11	15	t_{DB}	9, 10, 11
8	t_{WP}	9, 10, 11	16	t_{WR}	9, 10, 11
			17	t_{WPH}	9, 10, 11

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MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

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